Remarks

In the official action date October 24, 2003, the Examiner rejects claims 1 and 2 under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,592,468 to Sato. This ground for rejection is respectfully traversed.

MPEP 2131 states that a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," quoting *Verdegaal Bros v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

The Sato patent cited by the Examiner does not teach each and every element of claim 1 and therefore the rejection under 35 U.S.C. 102(b) is clearly improper and must be withdrawn.

It is noted that claim 1 is directed to a method of making block error rate measurements and includes the limitation of "opening and maintaining an information block flow by..."

As a first point, where is there any discussion whatsoever of either measuring a block error rate or maintaining an information block flow in the Sato patent?

It is believed that it is conventionally understood that a block error rate is an error rate that is indicative of the rate at which checking the data block's check sequences reveals the data block to be in error. See, for example, the description which occurs at page 3, lines 7-16 of the application as filed. Moreover, if the Examiner does a search on the Internet for the term "BLER" the Examiner will note that the term is also known in the art. See, for example, the definition at http://www.discdupe.org/i/bler.htm.

With respect to the Sato patent cited by the Examiner, where is there any discussion whatsoever of "block error rate" or, for that matter, "BLER"?

The Examiner refers the Applicant to column 18, lines 10-28. At those lines, Sato himself does not refer to a block error rate, but merely refers to an error rate (see, for example, line 10). However, the term "error rate" could refer to a whole variety of error rates other than a block error rate. Indeed, it is believed that that to which the Examiner refers is not a block error rate as conventionally understood and as described in the present application.

The Examiner attempts to remedy this deficiency by pointing to a parameter L, asserting that L is a measure of frame or block error rate. With all due respect to the Examiner, the Examiner's assertion is not based upon facts which are presented in Sato, but rather appear to be "facts" in the personal knowledge of the Examiner. If the Examiner is going to rely on "facts" within his own personal knowledge, then the Examiner is respectfully requested to comply with the rules of practice, particularly 37 CFR 1.104(d)(2) and to put his assertions into Affidavit form as required by the rules of practice. Either that, or the Examiner is requested to cite a prior art reference which supports his contentions.

Moreover, the Applicant respectfully submits that the assertions made by the Examiner with respect to parameter L are wrong. The Examiner asserts that "L is a measure of frame or block error rate". However, the prior art reference itself defines L as "a sum of packet lengths..." (emphasis added, see column 18, lines 20-22). As such, as the parameter L is defined in the Sato patent, it cannot possibly be a rate (i.e., a frequency of occurrence) when it is defined as being a sum of packet lengths!

Part of the problem with the Examiner's analysis appears to be that the Examiner makes incorrect assumptions as to exactly what the term block error rate means. This becomes particularly evident on page 5 of the official action where the Examiner asserts that the bit error rate BER could be calculated from the block error rate BLER with an "obvious formula" which the Examiner sets forth. With all due respect to the Examiner, the Applicant not only disagrees with the Examiner's assertions, but also objects to the manner by which the Examiner tries to introduce this "fact" into the prosecution of this application. First, it is submitted that the Examiner's assertions are, with all due respect,

erroneous. A simple example will make Applicant's point clear. A single erred bit in an N-bit data block causes the entire block to be in error, i.e., a single block error occurs. However, if all N-bits in the same N-bit data block are in error, that will also cause only a single block error, but the differences in the bit error rate differ by a factor N. Thus, there is not a linear relationship between the bit error rate and the block error rate. The simple formula advanced by the Examiner cannot possibly be correct.

Also, the Applicant objects, with all due respect to the Examiner, at the Examiner's attempt at introducing "facts" into the prosecution of this application without an appropriate evidentiary basis. The Examiner is respectfully requested to comply with the rules of practice by citing either prior art references supporting his contentions or, if the Examiner wishes to introduce facts within his own knowledge, then the Applicant will insist that the Applicant do so in accordance with the rules of practice, namely, in Affidavit form as specifically required by 37 CFR 1.04(d)(2).

The Examiner goes on to assert that Sato teaches "opening and maintaining an information block flow", referring to column 1, lines 15-31 of Sato. Where is there any discussion or reference to "opening and maintaining an information block flow by sending repeated message blocks..." as specifically recited by claim 1? It is submitted, with all due respect to the Examiner, that the Examiner reads more into Sato than what Sato teaches. Where is the notion of "sending repeated message blocks" as stated by the Examiner at page 3, line 2 of the official action, revealed in Sato? Of course, in packet systems and in other error correction communication schemes, packets or data can be repeated, when requested, for example, when the receiving party sends back an NACK message as opposed to an ACK message. However, claim 1 recites "opening and maintaining an information block flow by sending repeated message blocks..." In conventional ACK/NACK transport systems, the sender only repeats a message when it has to and therefore does not maintain "an information block flow by sending repeated message blocks" as specifically cited by claim 1.

So, even if one assumed, for the moment, that Sato taught a method of making block error rate measurements, how does Sato possibly meet the limitation quoted above?

Moving on to claim 2, claim 2 recites that "the message blocks have a predetermined characteristic which causes the message blocks to be discarded upon processing..." With respect to the Examiner's analysis regarding claim 2, there is nothing which the Examiner points to which teaches message blocks which have a predetermined characteristic which causes the message blocks to be discarded upon processing. That which causes message blocks to be discarded in the prior art is the fact that the message blocks or packets get scrambled in transmission. When they are scrambled in transmission, then they are discarded. However, the scrambling during transmission is not "a predetermined characteristic which causes the message blocks to be discarded" as specifically claimed in claim 2.

In terms of the present technology, as disclosed in the patent application, the Examiner is invited to turn to page 5 of the application and read lines 25-28. Note that the FCS is deliberately made incorrect, by calculating its inverse, and the incorrect FCS is attached to the rest of the data. By intentionally attaching an incorrect FCS, that causes the received data to be discarded. See also, page 6, lines 7-12 of the application as filed.

The application as filed teaches one way of providing a "predetermined characteristic" (intentionally attaching incorrect FCS in the disclosed embodiment) which causes the message blocks to be discarded upon processing. In the prior art cited by the Examiner, it appears that if a message block is received, as transmitted, then it is not discarded, whereas if there is an error in transmission, it is discarded. The error correction code in the prior art does not cause the message to be discarded. It is the error in transmission which causes the error to be discarded and the error detection code only permits the error to be detected. Thus, the detection code does not cause message blocks to be discarded, but rather permits faulty or erred message blocks to be detected. Where does any of the prior art cited by the Examiner teach, for example, intentionally sending an erroneous error detection code or intentionally sending erroneous data which causes the message block to be discarded?

The prior art cited by the Examiner clearly does not anticipate either claims 1 or 2. Moreover, with all due respect to the Examiner, the Applicant does not understand why

the Examiner attributes features to the prior art which it does not seemingly teach. For example, the way the Examiner discusses block error rate in the paragraph bridging pages 2 and 3 of the official action, one would think, therefrom, that block error rate was clearly taught by Sato. However, the Applicant can find no discussion whatsoever of block error rate being discussed in Sato.

Additionally, where does Sato teach "maintaining an information block flow by sending repeated message blocks" as required by claim 1? It is submitted in the prior art that data, such as packets, are resent when the sending station receives an NACK from the receiving station but not for "maintaining an information block flow" as recited in claim 1. Indeed, in communications systems, it is submitted that the prior art would teach trying to reduce the amount of repeated message blocks or packets which are sent as opposed to intentionally "maintaining an information block flow by sending repeated message blocks" as specifically claimed by claim 1. The Examiner's rejection of claims 1 and 2 under 35 U.S.C. 102 must fail since Sato fails to meet each and every limitation of those claims. Indeed, the Examiner admits as much at page 5 of the official action where the Examiner asserts that Sato "substantially teaches" the claimed invention in claims 1 and 2. While the Applicant denies that characterization since the Applicant believes that Sato is basically irrelevant to claims 1 and 2, the Examiner's assertion that Sato "substantially" teaches the invention argues against a rejection of those claims under 35 U.S.C. 102. In any event, for the reasons indicated by Applicant above, Sato is basically irrelevant to claims 1 and 2.

Turning briefly to the Examiner's analysis regarding claim 3, the Examiner asserts that it would somehow be obvious to combine Sato with US Patent No. 5,946,320 to Decker. The Examiner asserts that Decker teaches at column 4, lines 24-48 that BER measurements are required. If that is so, does that mean that the Sato disclosure is inoperable? If BER measurements are required, as asserted by the Examiner, then one would not be motivated to combine Sato with Decker since Sato teaches us nothing about BER measurements. Perhaps the Examiner meant to indicate that BER measurements are optional. If that is so, then why modify Sato, making Sato more complicated, in order to make BER measurements? Where exactly is the motivation for

making the combination asserted by the Examiner?

Moreover, the Examiner's assumptions with respect to the relationship between BER (the bit error rate) and BLER (the block error rate) has already been shown to be in error in the discussion set forth above with respect to claim 1, and the Examiner does not explain how Decker makes up for the shortcomings noted above with respect to Sato. Thus, even if it is assumed that it is somehow obvious to combine the teachings of Decker and Sato, the asserted combination does not render any of the claims in this application obvious.

The Applicant also has a few comments on the Examiner's discussion regarding inherency in the paragraph which bridges page 3 and 4 of the application. The Examiner asserts that the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill", quoting Continental Can Company USA v. Monsanto Co. It is submitted, with all due respect to the Examiner, that the Examiner made no showing whatsoever with respect to whether or not the propounded test is satisfied. As such, the rejection of claim 2 under 35 U.S.C. 102 must fail for that reason alone. Of course, the rejection also fails for the reasons set forth above with respect to claim 1 and the reasons set forth above with respect to claim 2 in that the cited documents fail to anticipate the language of claim 2.

Moreover, the Examiner seems to be of the impression that the Examiner is entitled to cite non-prior art references in the context of a 35 U.S.C. 102 rejection by introducing them as teaching references "for what is inherent in the art". What is inherent (today) in the art, is utterly irrelevant to the claims of a patent application which enjoys an earlier filing date. If the Examiner wants to make an inherency argument, for whatever reason, it is submitted that the Examiner has to rely on prior art references whether they are introduced to show inherency, obviousness or for some other reason. Clearly, the Examiner would be entitled to cite Matsunaga under 35 U.S.C. 102(e), but with respect to the article entitled "The Seven Layers of the OSAI Model", it appears that that document is undated. Since it is not particularly clear why the Examiner is bothering to

cite that document, the Applicant will hold in abeyance any possible objection it may have to that document until such time as the Examiner makes it clear as to why it is being cited and what material from it the Examiner wishes to rely upon.

However, the Applicant does wish to make it clear that the Applicant disagrees with the notion which seems to carry through the aforementioned paragraph that the Examiner is entitled to cite a document which does not qualify as a prior art reference by telling the Applicant, instead, that it teaches that which is inherent in the art. With all due respect to the Examiner, the Applicant rejects that notion.

Claim 4 recites that "the repeated message blocks are GMM_INFORMATION message blocks. With respect to the Examiner's reference to page 4, lines 1-3 of Applicant's application, there is no discussion at that point of "repeated message blocks" recited in claim 4, and therefore the Examiner's prior art analysis simply does not make sense. The Examiner points the Applicant to the Examiner's handling of claim 3, but there is no discussion of the repeated message blocks recited in claim 4. And, as indicated in the Applicant's review of the Sato patent cited by the Examiner, the Applicant could find no discussion of "maintaining an information block flow by sending repeated message blocks" in Sato. So, just what is the nexus between the repeated message blocks, which do not appear to be disclosed in the prior art cited by the Examiner, and the GMM_INFORMATION message blocks recited in claim 4? The passage to which the Examiner refers the Applicant at lines 1-3 of page 4 of Applicant's own patent application does not make the nexus. Rather, the Examiner seems to assume that the nexus somehow exists. Why? It is noted that this is a rejection under 35 U.S.C. 103 and the Examiner has the obligation of explaining to the Applicant just what is the motivation that one of ordinary skill in the art would have to make the invention as of the filing date of the application. That the Examiner does not do and therefore the rejection under 35 U.S.C. 103 must fail.

In making obviousness type prior art rejections, the test is what would have been obvious to one of ordinary skill in the art at the time the invention was made. For example, turn to the Examiner's rejection of claim 8. The Examiner states that "inclusion

in a message block of an invalid frame check sequence would inherently cause the message block to be discarded..." That sort of analysis, if correct, would lead to the invalidation of almost any invention. Claim 8 recites that "the predetermined characteristic comprises inclusion in a message block of an invalid frame check sequence." In the Examiner's handling of the rejection of claim 8, the Examiner basically assumes that the "inclusion in a message block of an invalid frame check sequence" is known in the prior art, without bothering to show where it is known in the prior art. The rules of practice make it clear that the Examiner is not entitled to assume that it is known in the prior art, but rather must make specific reference to a prior art reference (or produce an Affidavit) and when the Examiner points to prior art references, the Examiner has the obligation when the reference is complex or shows or describes inventions other than that claimed by the Applicant, to point out "as nearly as practicable" the "particular part relied upon". See 37 CFR 1.104(c )(2).

If the Examiner continues to reject any of the claims in this application on prior art grounds, then the Examiner is requested, as required by the rules of practice, to point out with specificity where each and every limitation of each rejected claim can be found in the prior art. If the Examiner wishes to rely upon information within his own purview, then the Examiner is specifically requested to either cite a prior art reference which supports his contentions or to support his contentions with an Affidavit, as required by the rules of practice.

It is believed, that upon reconsideration, the Examiner will agree that the prior art rejections made in the official action were made improvidently and should be withdrawn.

Reconsideration is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents POB 1450, Alexandria, VA 22313-1450 on

January 26, 2004

(Date of Deposit)

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